

**What is Claimed:**

1                    1.        A process for manufacturing an integrated circuit package  
2 comprising:

3                    (a)        providing a substrate having a first dielectric layer, a conductive  
4 layer above the first dielectric layer, and a second dielectric layer above the conductive  
5 layer, the second dielectric layer having a cavity exposing a portion of the conductive  
6 layer; and

7                    (b)        interconnecting an integrated circuit directly to the exposed portion  
8 of the conductive layer in the cavity.

1                    2.        The method of claim 1 wherein step (b) comprises:  
2 coupling a conductor to a bond pad formed on the integrated circuit; and  
3 connecting the conductor directly to the conductive layer.

1                    3.        The method of claim 1 further comprising providing one of a  
2 ground plane and a power plane in the exposed portion of the conductive layer.

1                    4.        The method of claim 3 further comprising providing at least one  
2 connection for a signal line in the exposed portion of the conductive layer.

1                    5.        The method of claim 1 further comprising providing at least one  
2 connection for a signal line in the exposed portion of the conductive layer.

1                    6.        The method of claim 1 further comprising forming multiple  
2 interconnections between the integrated circuit chip and the conductive layer.

1                    7.        A method of manufacturing a substrate adapted to receive an  
2 integrated circuit chip comprising:

3                    (a)        providing a first dielectric layer;

4                    (b)        providing a conductive layer above the first dielectric layer;

5                    (c)        providing a second dielectric layer above the conductive layer; and

6                    (d) forming a cavity in the second dielectric layer to expose a portion of  
7 the conductive layer.



1                    8.     The method of claim 7 wherein steps (a), (b), and (c) occur prior to  
2     step (d).

1                    9.     The method of claim 7 further comprising:  
2                    providing a contact area to a ground plane by exposing the portion of the  
3     conductive layer.

1                    10.    The method of claim 7 further comprising:  
2                    (e) forming plated through holes in the substrate.

1                    11.    The method of claim 10 wherein step (e) is performed prior to step  
2     (d).

1                    12.    A method of manufacturing an integrated circuit package  
2     comprising:  
3                    providing the substrate of claim 7; and  
4                    coupling the integrated circuit chip to the substrate.

1                    13.    A method of manufacturing a substrate adapted to receive an  
2     integrated circuit chip comprising:

3                    (a)    providing a first dielectric layer;  
4                    (b)    providing a first conductive layer above the dielectric layer;  
5                    (c)    providing a second dielectric layer above the first conductive layer;  
6                    (d)    providing a second conductive layer above the second dielectric  
7     layer;

8                    (e) forming a cavity in a first region of the second dielectric layer to  
9     expose a portion of the first conductive layer.

1                    14.    The process of claim 13 wherein step (d) further comprises  
2     providing the second conductive layer on regions other than the first region.

1                    15.    The process of claim 13 wherein step (d) further comprises  
2     removing a portion of the conductive layer formed above the first region.

1                    16.    A method of manufacturing an integrated circuit package  
2     comprising:

Sub A 31  
Sub A 44  
Sub A 49



4 coupling the integrated circuit chip to the substrate.

7 (a) receiving a substrate having a first dielectric layer, a conductive  
8 layer above the first dielectric layer, and a second dielectric layer above the conductive  
9 layer, the second dielectric layer having a cavity exposing a portion of the conductive  
10 layer; and

11 (b) interconnecting an integrated circuit directly to the exposed portion  
12 of the conductive layer in the cavity.

Year	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	